METHOD AND SYSTEM FOR DIVIDING CONFIGURATION SPACE

CROSS-REFERENCE TO RELATED APPLICATION

This application claims the priority benefit of Taiwan application serial no. 90108178, filed on April 4, 2001.

BACKGROUND OF THE INVENTION

Field of the Invention

[0001] The invention relates in general to a design of configuration space. More particularly, the invention relates to a method of dividing a configuration space.

Description of the Related Art

[0002] A north bridge control chip and a south bridge control chip normally exist in a conventional computer system using the PCI bus. Figure 1 shows a conventional PCI bus system structure and the distributed locations of the configuration spaces thereof. In Figure 1, in a PCI bus system, a north bridge control chip 100 comprises a configuration space for host bridge 160. The configuration values of the microprocessor 110, the memory system 150 and the PCI bus 120 are stored in the registers of the configuration space for host bridge 160. Similarly, the south bridge control chip 130 comprises a configuration space for the ISA bridge 190 to store the configuration values required by the peripherals connected to the south bridge control chip. In Figure 1, the north bridge control chip 100 is responsible for connecting the microprocessor 110 and a 33MHz PCI bus 120, while the south bridge control chip 130 is responsible for connecting the peripherals such as the USB controller and the IDE controller to the 33MHz PCI bus 120.

A LAN controller may also use the 33MHz PCI bus to connect a memory system such as a DRAM. As the transmission speed of the memory bus and the peripherals is increased, a bottleneck of data transmission speed falls on the PCI bus with only a speed of 33MHz.

SUMMARY OF THE INVENTION

[0003] The invention provides a method of distribution and storage of a configuration space that can be applied to an advanced computer system without modifying the BIOS or system software used in the conventional computer system. That is, for the BIOS or OS system development, the advanced computer system does not have any change in the access method and structure of configuration.

[0004] A method of dividing a configuration space is provided by the invention. The method can be applied to a computer system using a PCI bus, especially to an advanced computer system that quotes a high speed private bus between a north bridge control chip and a south bridge control chip. The computer system comprises a microprocessor, a host bus, the north bridge control chip, the high speed private bus, a PCI bus, the south bridge control chip, a memory bus, and a memory system. The host bus connects the microprocessor to the north bridge control chip. The high speed private bus is responsible for connecting the north bridge control chip to the south bridge control chip. Using the south bridge control chip, the PCI bus is connected to the host bus or the memory bus via the high speed private bus. The method provides an actual configuration space A stored in the north bridge control chip to store the configuration value relating to the microprocessor and the memory system. The method also provides an actual configuration storage space B in the south bridge control chip to store the configuration value relating to the PCI bus. In addition, the method provides a duplicated copy of

configuration storage space B(A) in the north bridge control chip (south bridge control chip). Such duplicated copy of configuration storage space is an empty configuration space. The method further provides a selector in the north bridge control chip to select data to be read according to the specific requirement.

[0005] When the microprocessor intends to perform an operation of writing a configuration value, and if the data is to be written into the actual storage configuration space A of the north bridge control chip, the north bridge control chip executes the write operation. Meanwhile, the north bridge control chip also informs the south bridge control chip that the data is written into the duplicated copy of configuration space A of the south bridge control chip. If the data is written into the actual configuration storage space B of the south bridge control chip, in addition to send the write request to the south bridge control chip, the north bridge control chip also executes a write operation on the duplicated copy of configuration space B of the north bridge control chip. If the microprocessor is to perform a read operation on the configuration data, the read request is sent to both the north and south bridge control chips. Meanwhile, according to the read address, the selector located in the north bridge control chip determines such data is obtained from either the actual configuration space A of the north bridge control chip, or the actual configuration space B of the south bridge control chip.

[0006] Thus, to the microprocessor, it seems that all the configuration data are stored in the north bridge control chip. But actually, some configuration values related to the PCI bus are stored in the south bridge control chip. The design can conceal the influence caused by the quotation of a high speed private bus in the advanced computer system, but meet the requirement of dividing the configuration space distribution in the advanced system.

[0007] For the BIOS or OS system, the configuration space is equivalently undivided such that the original software program does not have to be modified correspondingly. But in fact, the configuration space is stored in the north bridge control chip and the south bridge control chip according to the specific requirement, respectively. The advanced computer system can thus quote a high speed private bus between the north and south bridge control chips to enhance the transmission functions.

[008] Both the foregoing general description and the following detailed description are exemplary and explanatory only and are not restrictive of the invention, as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] Figure 1 shows a system structure and the distribution locations of configuration spaces of a PCI bus;

[0010] Figure 2 shows another system structure and the distribution locations of configuration spaces of a PCI bus; and

[0011] Figure 3 shows a system structure and the distribution locations of configuration spaces of a PCI bus according to the invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0012] To increase the transmission speed, a high speed private bus is introduced between a south bridge control chip and a north bridge control chip of the advanced computer system. The previous PCI bus with 33 MHz is shifted into the south bridge control chip. In a co-pending US patent applications Nos. 09/718,811 and 09/735,412, which the inventor of the invention is one of the co-inventors, a high speed private bus is

used for the data transmission between the north and south bridge control chips. When the speed of the peripherals of the south bridge control chip is enhanced, the data transmission is not restricted to 33 MHz of the PCI bus since the data can be transmitted via the high speed private bus. Figure 2 shows a system structure having the private bus and the distribution locations of configuration spaces of a PCI bus. As shown in Figure 2, the north bridge control chip 100 is responsible for the connection between the microprocessor 110 and the high speed private bus 140. The south bridge control chip 130 is responsible for the connection between the high speed private bus 140 and the PCI bus 120 and other peripherals.

[0013] For the substantial structure, this sort of advanced system requires a main connector in the north bridge control chip responsible for the data transmission between the microprocessor and the high speed private bus. An additional connector is also required in the south bridge control chip for the data transmission between the high speed private bus and the PCI bus. The south bridge control chip also comprises an ISA bus connector. Such variation affects the BIOS or the OS system since all the paths from the microprocessor to the PCI bus 120, the ISA bus 180 and other peripherals have to go through the additional connectors in the north and south bridge control chips.

[0014] As mentioned above, in the advanced computer system, a high speed private bus is introduced between the north bridge control chip and the south bridge control chip to increase the data transmission speed. The PCI bus 120 is shifted to the south bridge control chip 130. As shown in Figure 2, a first part of the configuration space for host bridge 160 located in the north bridge control chip 100. A second part of the configuration space for host bridge 170, which originally located in the north bridge control chip, has to be shifted into the south bridge control chip 130. That is, the

configuration values of the configuration space for host bridge 170 related to the PCI bus 120 has to be stored in the south bridge control chip. In order to apply to the advanced computer system, some modification of the previous software should be done, but it will cause an extra burden for the development of BIOS or OS.

[0015] Figure 3 shows a system structure of a PCI bus and the distribution location of the configuration spaces according to the invention. As shown in Figure 3, a system of dividing the configuration space is provided. The system comprises a microprocessor 110, a host bus 200, a north bridge control chip 100, a high speed private bus 140, a PCI bus 120, a south bridge control chip 130, a memory bus 210, and a memory system 150. The host bus 200 is responsible for the connection between the microprocessor 110 and the north bridge control chip 100. The memory bus 210 is responsible for the connection between the north bridge control chip 100 and the memory system 150. In addition, the newly introduced high speed private bus 140 connects the north and south bridge control chips 100 and 130. Using the south bridge control chip 130, the PCI bus 120 communicates with the host bus 200 or the memory bus 210 via the high speed private bus 140.

[0016] In the invention, the north bridge control chip 100 comprises an actual configuration space for host bridge A (220) to store the configuration values, which relates to the microprocessor 110 and the memory system 150, in the registers. The south bridge control chip 130 comprises an actual configuration space for host bridge B (250) to store the configuration values, which relates to the PCI bus, in the registers. In addition, there exists a configuration space for host bridge B (230) of the north bridge control chip 100 as a duplicated copy of the configuration space for host bridge B 250. The south bridge control chip 130 also has configuration space for host bridge A (240) as a

duplicated copy of the configuration space for host bridge A (220). Furthermore, the duplicated copy of the configuration spaces for host bridge B (230) and A (240) are empty configuration spaces. The north bridge control chip 100 further comprises a selector 260 selected by a SEL_NB signal. To respond the request from the microprocessor 110, the selector 260 selects either the configuration space for host bridge A (220) or the configuration space for host bridge B (250).

[0017] That is, when the microprocessor 110 is performing a read operation cycles on the target addressed to the configuration space for host bridge A (220), the real output data is selected from the actual configuration space for host bridge A (220) even though the configuration space for host bridge A (240) outputs a read data via the private bus. When the microprocessor 110 is performing a read operation cycles on the target addressed to the configuration space for host bridge B (250), the real output data is selected from the actual configuration space for host bridge B (250) via the private bus even though the configuration space for host bridge B (230) outputs a read data..

[0018] When the microprocessor 110 is performing a write operation on the configuration space for host bridge A (220), the north bridge control chip 100 also activates a write request to the south bridge control chip 130. However, such data is not really stored in the south bridge control chip 130, but is only stored in the configuration space for host bridge A (240), an empty configuration space. Similarly, if the data to be written by the microprocessor 110 is to be stored in the configuration space for host bridge B (250), the north bridge control chip 100 also writes the data into the configuration space for host bridge B (230), an empty configuration space. Meanwhile, the south bridge control chip 130 is requested to save the data into the configuration space for host bridge B (250) thereof.

[0019] That is, when the microprocessor 110 is performing a write operation cycle related to the configuration storage space, the write operation cycle is sent to both the north bridge control chip 100 and the south bridge control chip 130. When the target for the write operation cycle is addressed to the configuration space for host bridge A (220), the data is written into the actual configuration space for host bridge A (220) only. When the target for the write operation cycle is addressed to the configuration space for host bridge B (250), the data is written into the actual configuration space for host bridge B (250) only.

[0020] Thus, from the developers of BIOS or OS system point of view, the configuration space is equivalently undivided. The original software program can be applied without being modified. In fact, the configuration values are stored in registers of the north and south bridge control chips 100 and 130 according to specific requirements, respectively. As a result, a high speed private bus 140 can be used between the north and south bridge control chips to enhance the transmission speed.

[0021] Other embodiments of the invention will appear to those skilled in the art from consideration of the specification and practice of the invention disclosed herein. It is intended that the specification and examples be considered as exemplary only, with a true scope and spirit of the invention being indicated by the following claims.